In the Claims.

Please cancel claims 1-32.

- 5 33. (New) A random access memory cell, comprising:
 - a data storage node; and
 - a pass transistor coupled to provide charge transfer to and from the data storage node and including
 - a source region,
- a drain region,
 - a channel region disposed between the source region and the drain region, the channel region including a first channel side and a second channel side opposite to the first channel side,
 - a first channel side control gate, and
 - a second channel side control gate wherein
 - the first channel side control gate is formed in a trench.
 - 34. (New) The random access memory cell of claim 33, further including:
 - a substrate insulator layer providing electrical isolation between the first channel side control gate and a substrate.
 - 35. (New) The random access memory cell of claim 33, further including:
 - a first channel side gate insulating layer disposed between the first channel side control gate and the first channel side.

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36.	(New)	The random	access memor	v cell of	claim 35.	wherein:
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the first channel side gate insulating layer include thermally grown silicon dioxide.

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37. (New) The random access memory cell of claim 33, wherein:

the first channel side control gate includes doped polysilicon.

38. (New) The random access memory cell of claim 33, wherein:

a second channel side gate insulating layer disposed between the second channel side control gate and the second channel side.

39. (New) The random access memory cell of claim 38, wherein:

the second channel side gate insulating layer include thermally grown silicon dioxide.

40. (New) The random access memory cell of claim 33, wherein:

the data storage node includes polysilicon.

20 41. (New) The random access memory cell of claim 33, wherein:

the first channel side gate and the second channel side gate are electrically connected to a word line; and

the word line is electrically connected to a word line driver.

42 . (New)	The random	access memory cell of claim 33, wherein:						
	the data	storage	node is a	first to	erminal	of a sto	rage	capacitor.

- **43**. (New) The random access memory cell of claim 42, wherein:
- 5 the storage capacitor includes a capacitor dielectric layer including nitride.
 - **44**. (New) The random access memory cell of claim 42, wherein:

the storage capacitor includes a capacitor dielectric layer including Si_3N_4 .

- 45. (New) The random access memory cell of claim 42, wherein:

 the storage capacitor includes a capacitor dielectric layer including Ta₂O₅.
- 46. (New) The random access memory cell of claim 42, wherein:

 the storage capacitor includes a capacitor dielectric layer including SrTiO₃.
- 47. (New) The random access memory cell of claim 42, wherein:

the storage capacitor includes a capacitor dielectric layer including BaSrTiO₃.

48. (New) The random access memory cell of claim 42, wherein:

the storage capacitor includes a second terminal shared with at least another storage capacitor of another random access memory cell.

- 15 **49**. (New) The random access memory cell of claim 42, wherein:
 - the storage capacitor is a trench capacitor.
 - **50**. (New) The random access memory cell of claim 42, wherein:

the storage capacitor has a capacitor-over-bit line structure.

51. (New) The random access memory cell of claim 42, wherein:

the storage capacitor has a capacitor-under-bit line structure.

52. (New) The random access memory cell of claim 33, wherein:

the pass transistor is coupled to provide charge transfer between the storage node and a bit line; and

the bit line includes metal from the group consisting of Ti, Al, and Cu.

53. (New) The random access memory cell of claim 33, wherein:

the trench is at least partially defined by the substrate insulator layer.